AMENDMENTS TO THE SPECIFICATION

Please delete the originally-submitted Abstract and replace it with the following Abstract:

A clock and data recovery circuit including a phase synchronization loop including an oscillator, the oscillation frequency of which is variably controlled, the phase synchronization loop performing phase-synchronization of a clock signal output from the oscillator with an input data signal. The circuit also includes a discriminator circuit, responsive to a clock signal for discrimination, for discriminating the input data signal and outputting the discriminated signal. The circuit further includes a phase detector circuit for detecting the phase difference between an output data signal, discriminated and output by the discriminator circuit, and the input data signal. The circuit also includes a phase shift circuit for shifting the phase of the clock signal, output from the oscillator, based on a comparison result output from the phase detector circuit. The clock signal, which is output from the phase shift circuit, is supplied as the clock signal for discrimination to the discriminator circuit.